

Figure 1.3

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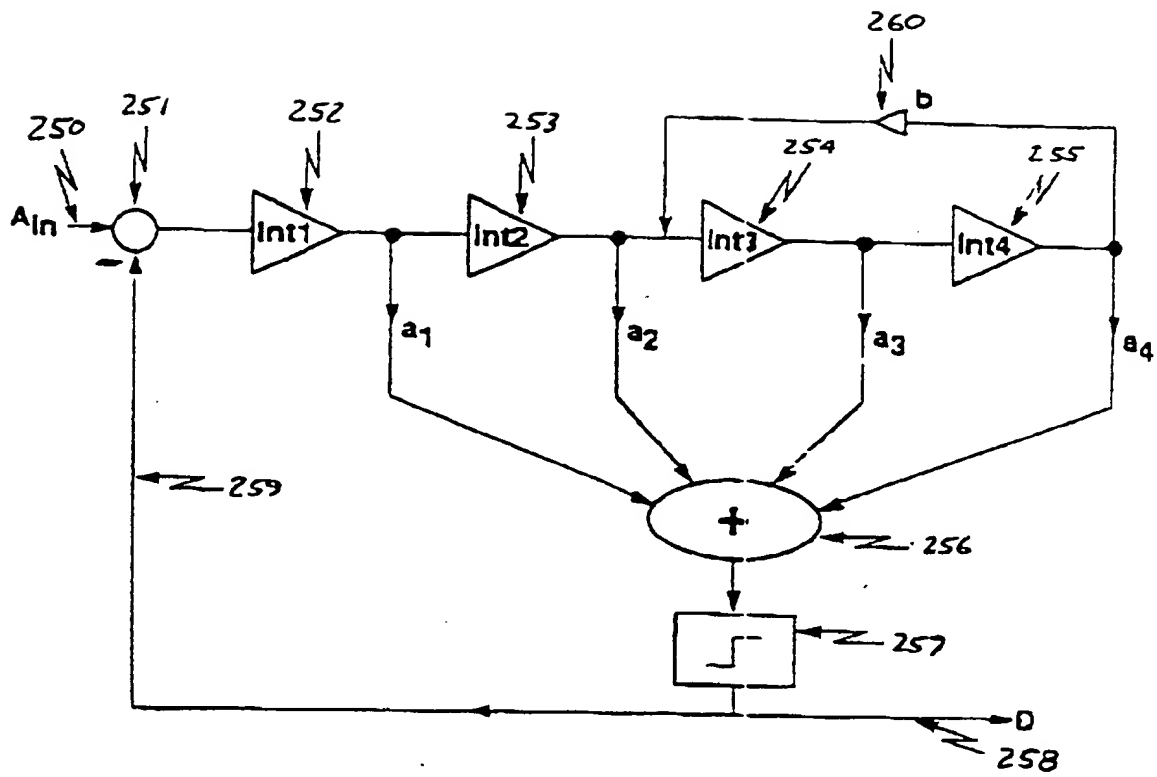


Figure 1.4

# DIGITAL BLOCK DIAGRAM

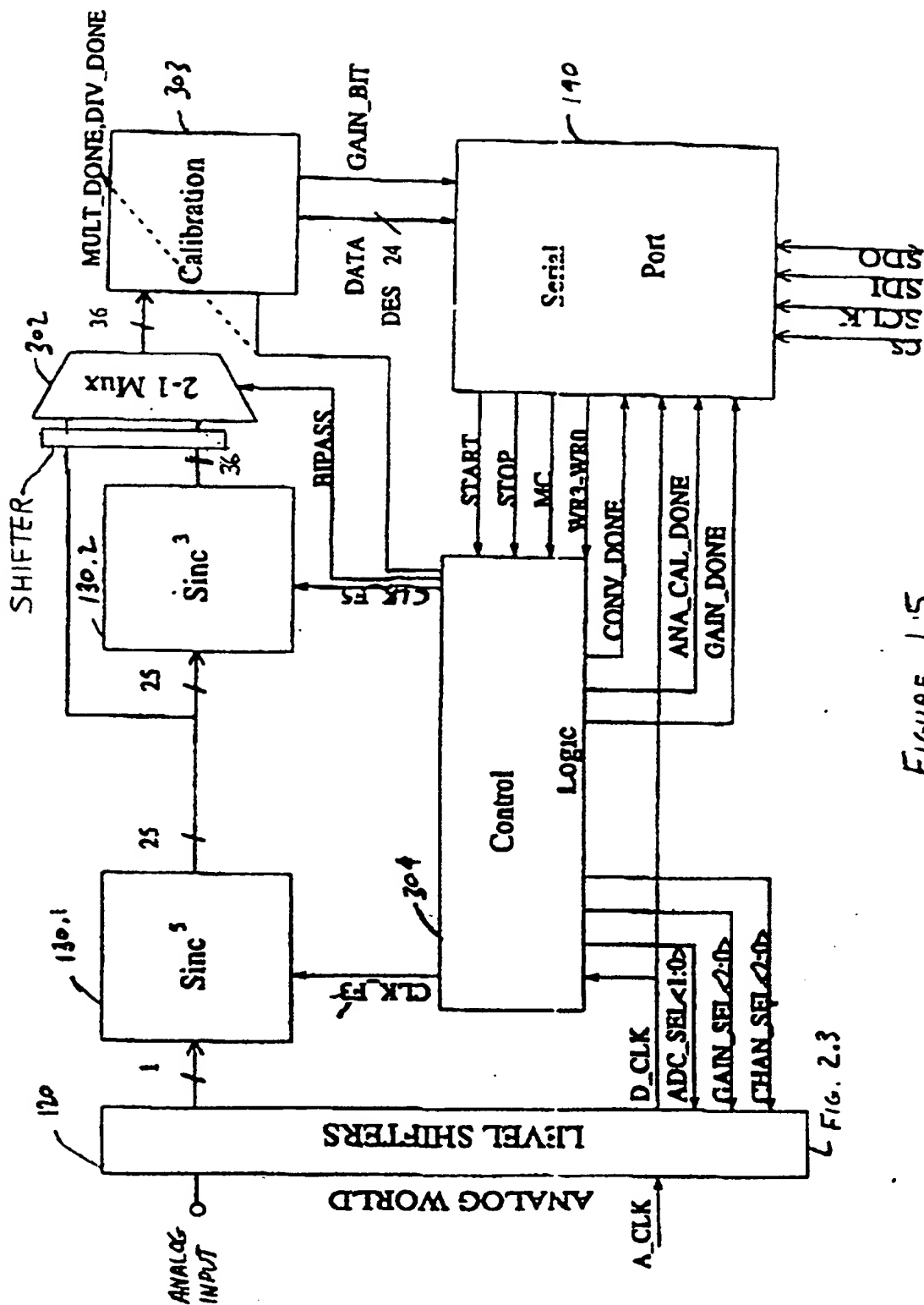


FIG. 2.3

FIGURE 1.5

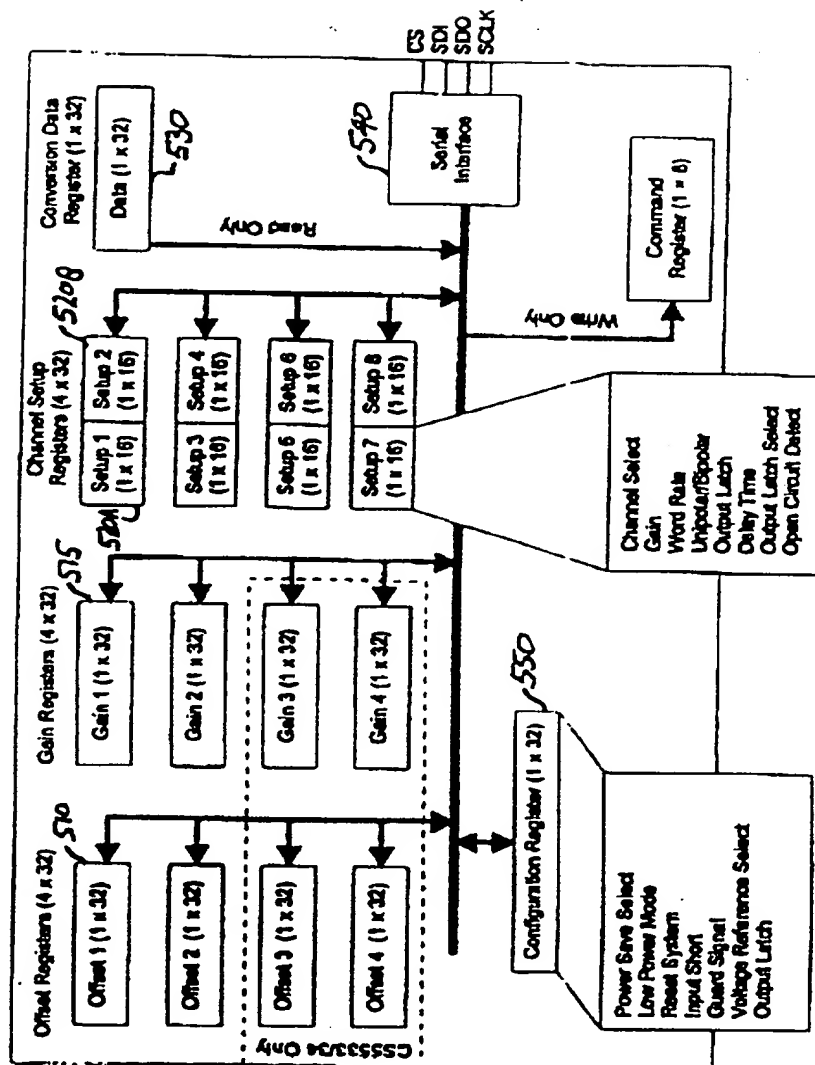


FIGURE 1.6

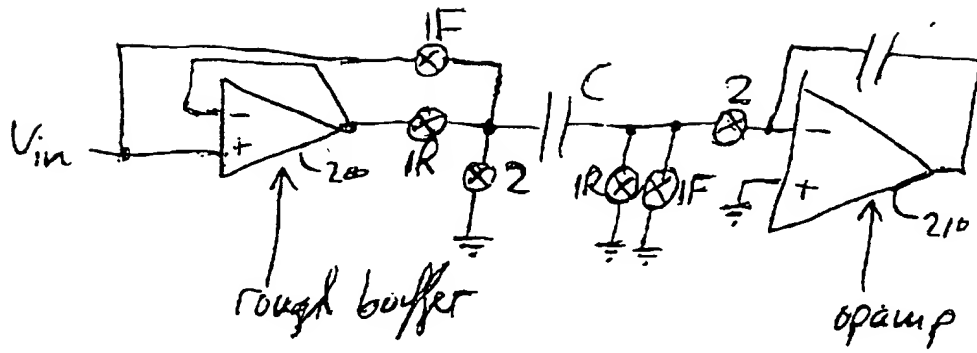


FIGURE 2.0

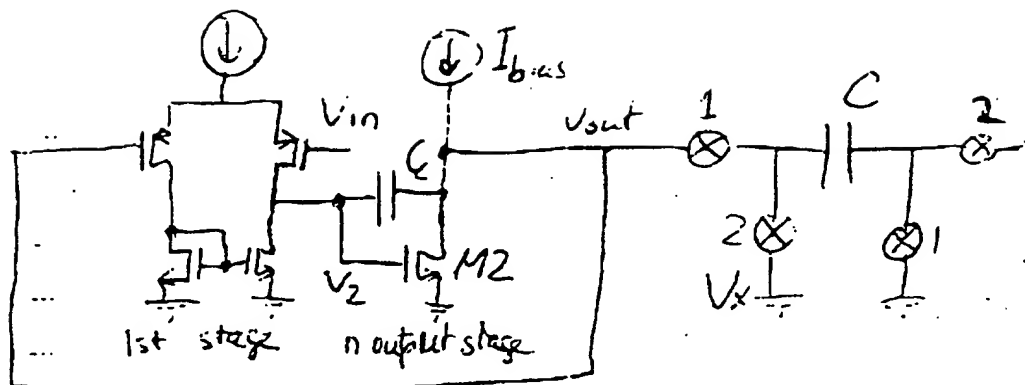


FIGURE 2.1



$V_{IN} = \text{CONSTANT}$

$V_{OUT} > V_X$

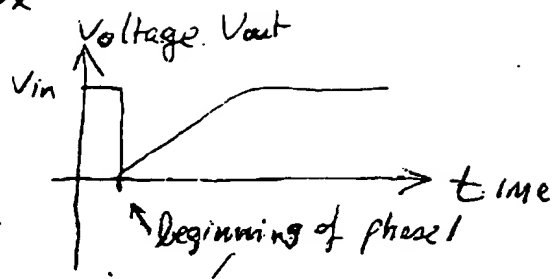


FIGURE 2.2

$V_{IN} = \text{CONSTANT}$

$V_{OUT} < V_X$

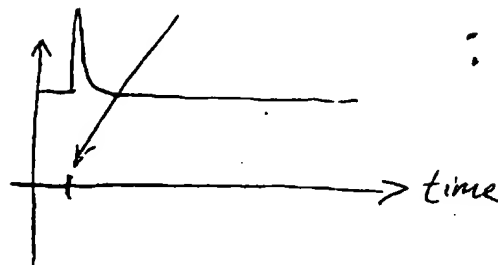


FIGURE 2.3

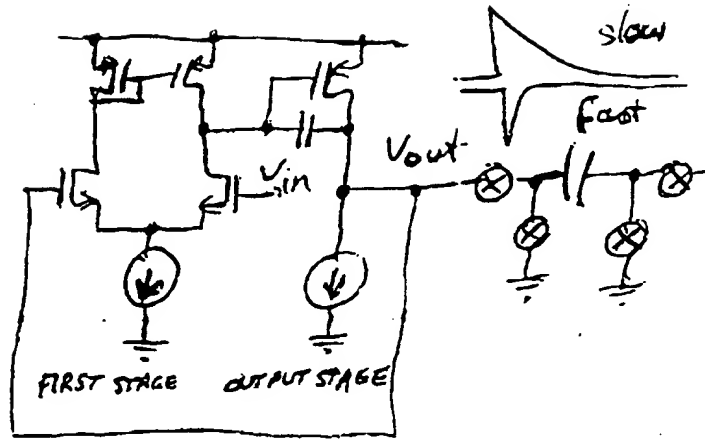


FIGURE 2.4

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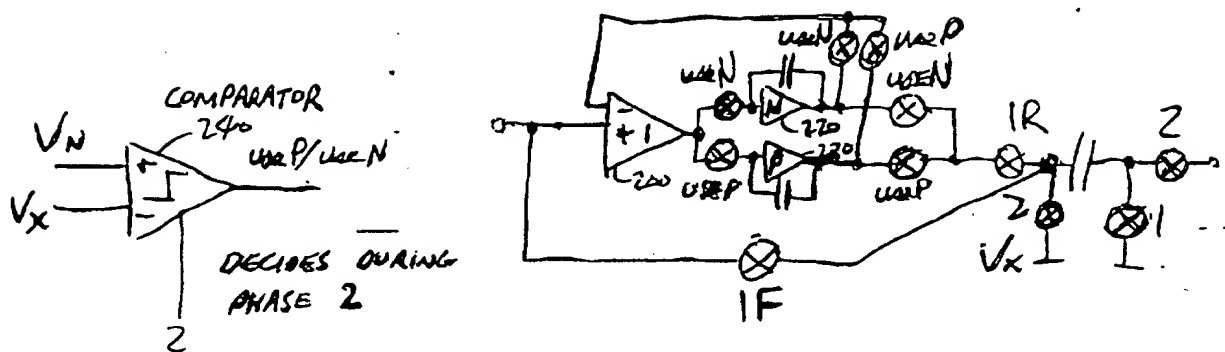


FIGURE 2.5

FIGURE 2.6

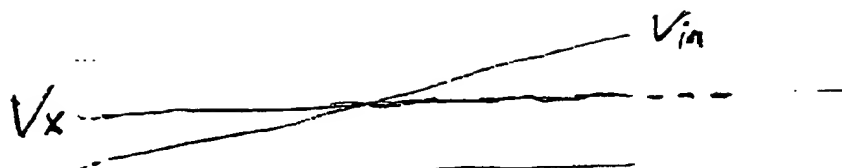


FIGURE 2.7

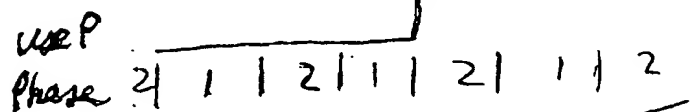
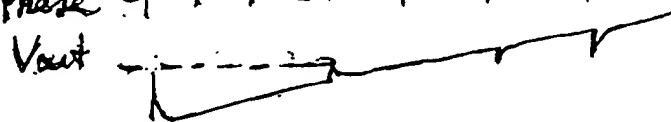


FIGURE 2.8



# MULTIPLIER ARCHITECTURE

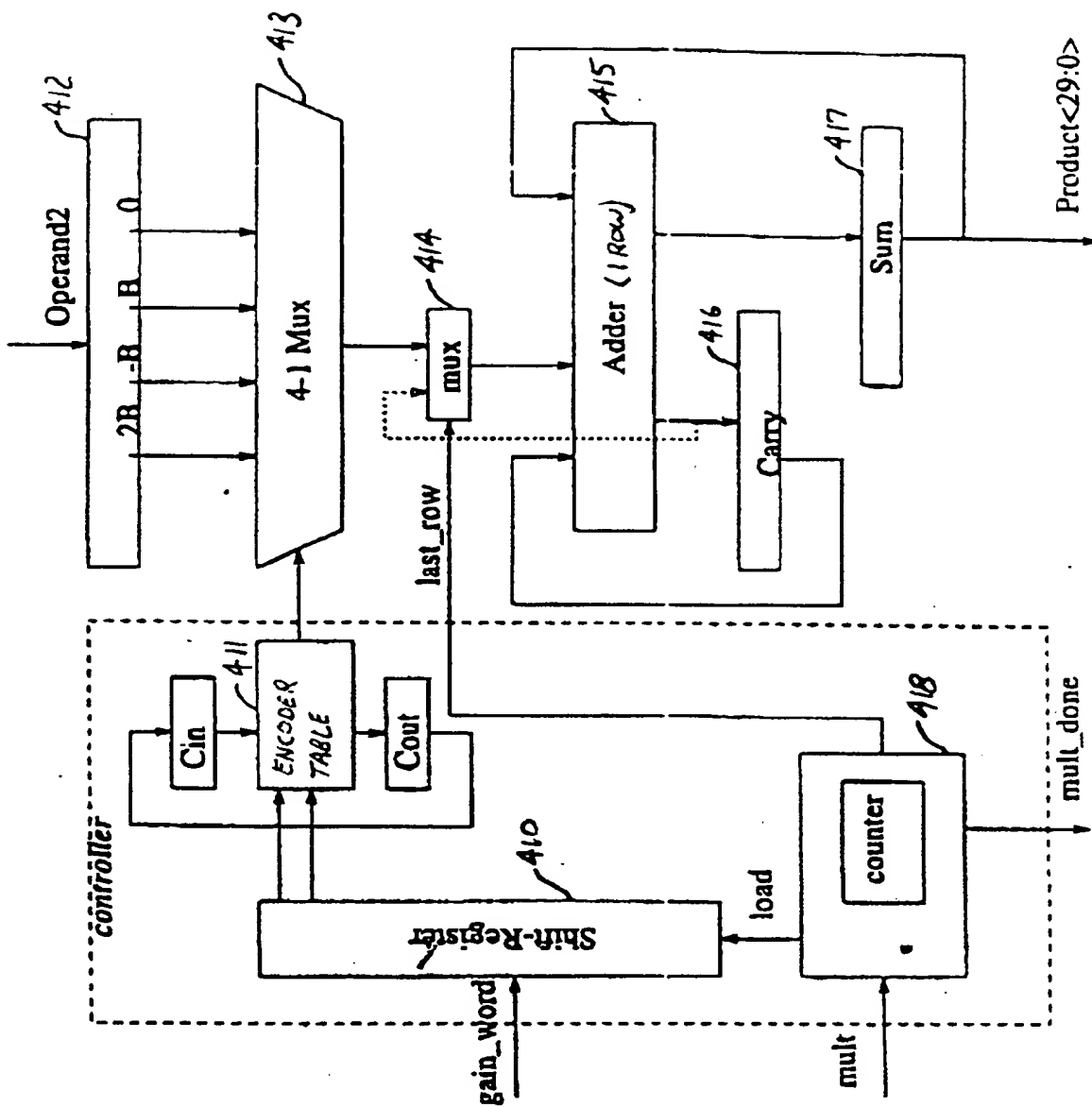


FIGURE 3.1

# Multiplication

FIGURE 3.2  
(PRIOR ART)

Table 2: Encoding Scheme Proposed

| $A_{i+1}$ | $A_i$ | Operation                |
|-----------|-------|--------------------------|
| 0         | 0     | $R_i = R_{i-1}/4$        |
| 0         | 1     | $R_i = (R_{i-1} + B)/4$  |
| 1         | 0     | $R_i = (R_{i-1} + 2B)/4$ |
| 1         | 1     | $R_i = (R_{i-1} + 3B)/4$ |

FIGURE 3.3  
(PRIOR ART)

Table 3: Carry Propagate Encoding Scheme

| $C_{in}$ | $A_{i+1}$ | $A_i$ | Operation                | $C_{out}$ |
|----------|-----------|-------|--------------------------|-----------|
| 0        | 0         | 0     | $R_i = R_{i-1}/4$        | 0         |
| 0        | 0         | 1     | $R_i = (R_{i-1} + B)/4$  | 0         |
| 0        | 1         | 0     | $R_i = (R_{i-1} + 2B)/4$ | 0         |
| 0        | 1         | 1     | $R_i = (R_{i-1} - B)/4$  | 1         |
| 1        | 0         | 0     | $R_i = (R_{i-1} + B)/4$  | 0         |
| 1        | 0         | 1     | $R_i = (R_{i-1} + 2B)/4$ | 0         |
| 1        | 1         | 0     | $R_i = (R_{i-1} - B)/4$  | 0         |
| 1        | 1         | 1     | $R_i = (R_{i-1})/4$      | 1         |

# Multiplication

FIGURE 3.4

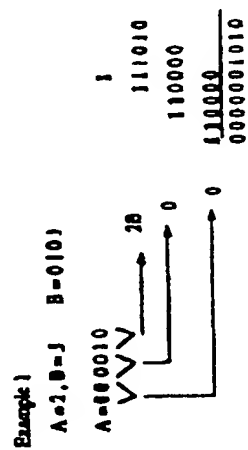
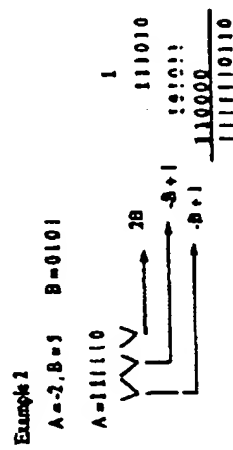


FIGURE 3.5



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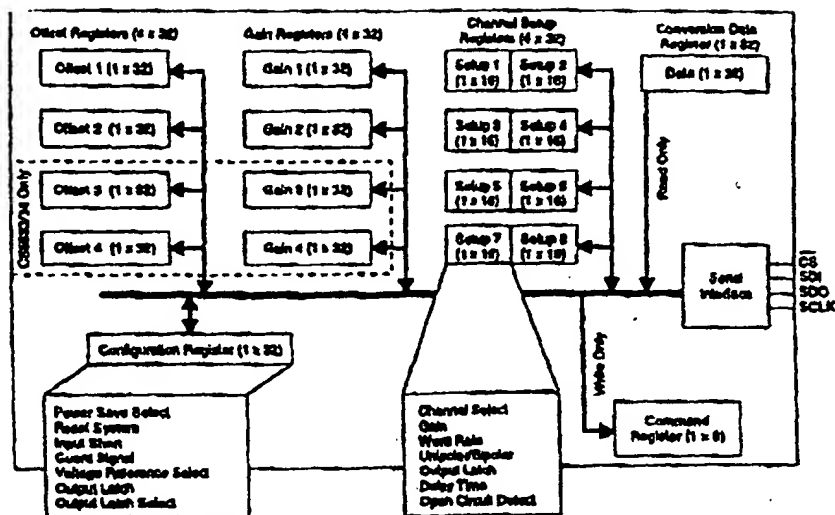


FIGURE 4.1



| D7(MSB) | D6  | D5  | D4  | D3  | D2   | D1   | D0   |
|---------|-----|-----|-----|-----|------|------|------|
| 0       | ARA | CS1 | CS0 | R/W | RSB2 | RSB1 | RSB0 |

| BIT   | NAME                            | VALUE | FUNCTION  |
|-------|---------------------------------|-------|---|
| D7    | Command Bit, C                  | 0     | Must be logic 0 for these commands.   |
|       |                                 | 1     | These commands are invalid if this bit is logic 1.  |
| D6    | Access Registers as Arrays, ARA | 0     | Ignore this function.   |
|       |                                 | 1     | Access the respective registers, offset, gain, or channel-setup, as an array of registers. The particular registers accessed are determined by the RS bits. The registers are accessed MSB first with physical channel 0 accessed first followed by physical channel 1 next and so forth. |
| D5-D4 | Channel Select Bits, CS1-CS0    | 00    | CS1-CS0 provide the address of one of the two (four for CS5533/34) physical input channels. These bits are also used to access the calibration registers associated with the respective physical input channel. Note that these bits are ignored when reading data register.              |
|       |                                 | 01    |   |
|       |                                 | 10    |   |
|       |                                 | 11    |   |
| D3    | Read/Write, R/W                 | 0     | Write to selected register.   |
|       |                                 | 1     | Read from selected register.  |
| D2-D0 | Register Select Bit, RSB3-RSB0  | 000   | Reserved  |
|       |                                 | 001   | Offset Register   |
|       |                                 | 010   | Gain Register   |
|       |                                 | 011   | Configuration Register  |
|       |                                 | 100   | Conversion Data Register (Read Only)  |
|       |                                 | 101   | Channel-Setup Registers   |
|       |                                 | 110   | Reserved  |
|       |                                 | 111   | Reserved  |

FIGURE 4.2

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| D7(MSB) | D6 | D5    | D4    | D3    | D2  | D1  | D0  |
|---------|----|-------|-------|-------|-----|-----|-----|
| 1       | MC | CSRP2 | CSRP1 | CSRP0 | CC2 | CC1 | CC0 |

| BIT   | NAME                                      | VALUE | FUNCTION   |
|-------|---|-------|--|
| D7    | Command Bit, C                            | 0     | These commands are invalid if this bit is logic 0.   |
|       |   | 1     | Must be logic 1 for these commands.  |
| D6    | Multiple Conversions, MC                  | 0     | Perform fully settled single conversions.  |
|       |   | 1     | Perform conversions continuously.  |
| D5-D3 | Channel-Setup Register Pointer Bits, CSRP | 000   | These bits are used as pointers to the Channel-Setup registers. Either a single conversion or continuous conversions are performed on the channel setup register pointed to by these bits. |
|       |   | ...   |  |
|       |   | 111   |  |
| D2-D0 | Conversion/Calibration Bits, CC2-CC0      | 000   | Normal Conversion  |
|       |   | 001   | Self-Offset Calibration  |
|       |   | 010   | Self-Gain Calibration  |
|       |   | 011   | Reserved   |
|       |   | 100   | Reserved   |
|       |   | 101   | System-Offset Calibration  |
|       |   | 110   | System-Gain Calibration  |
|       |   | 111   | Reserved   |

FIGURE 4.3

005201 90756950

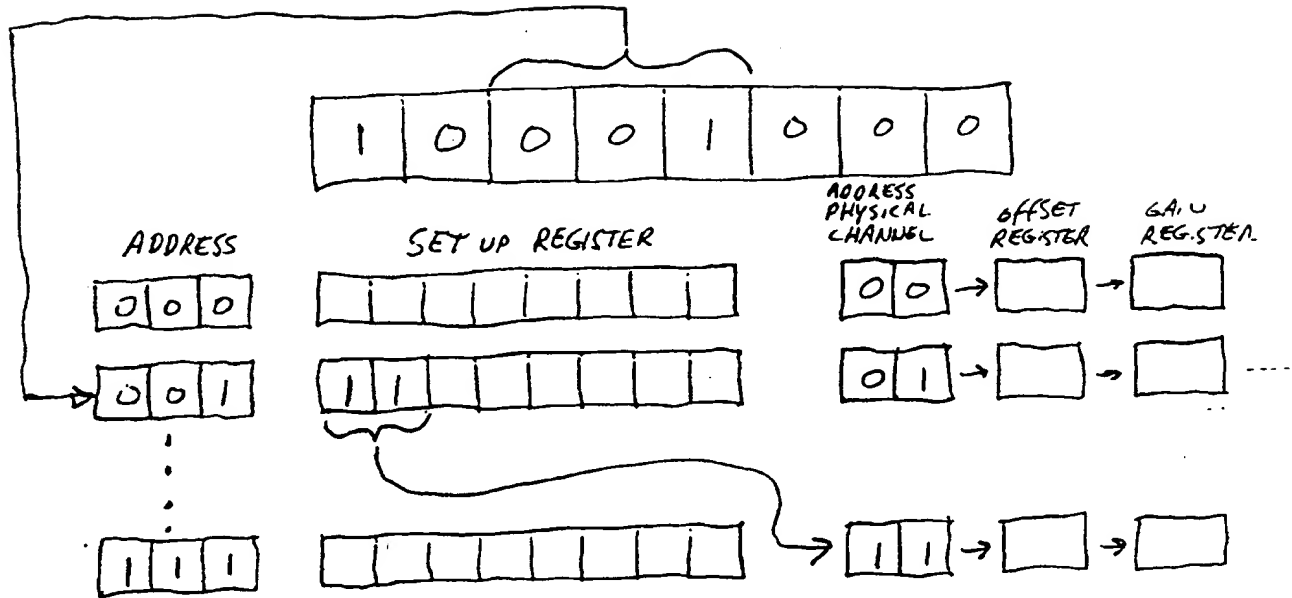


FIGURE 4.4

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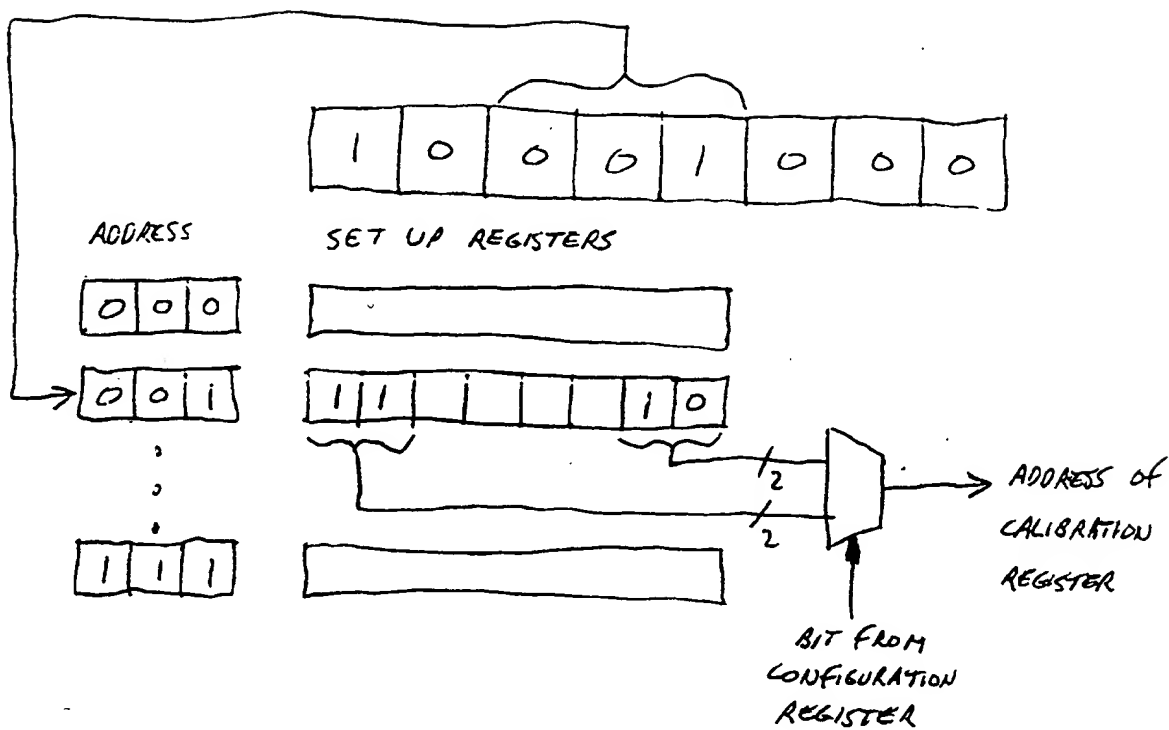


FIGURE 4.5

005207 90256950

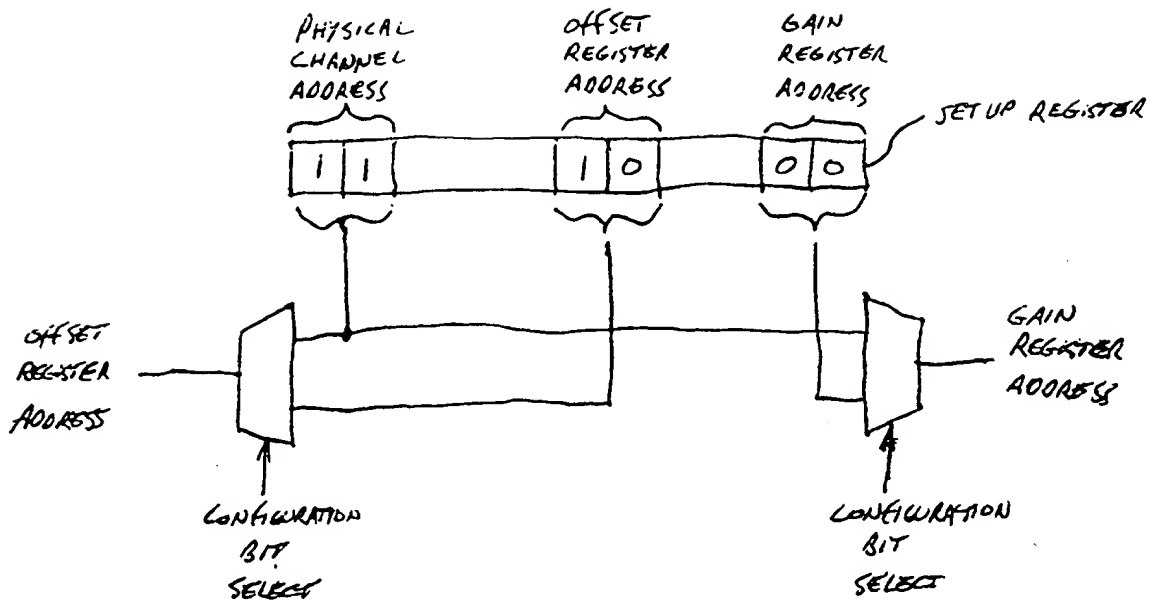
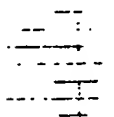


FIGURE 4.6



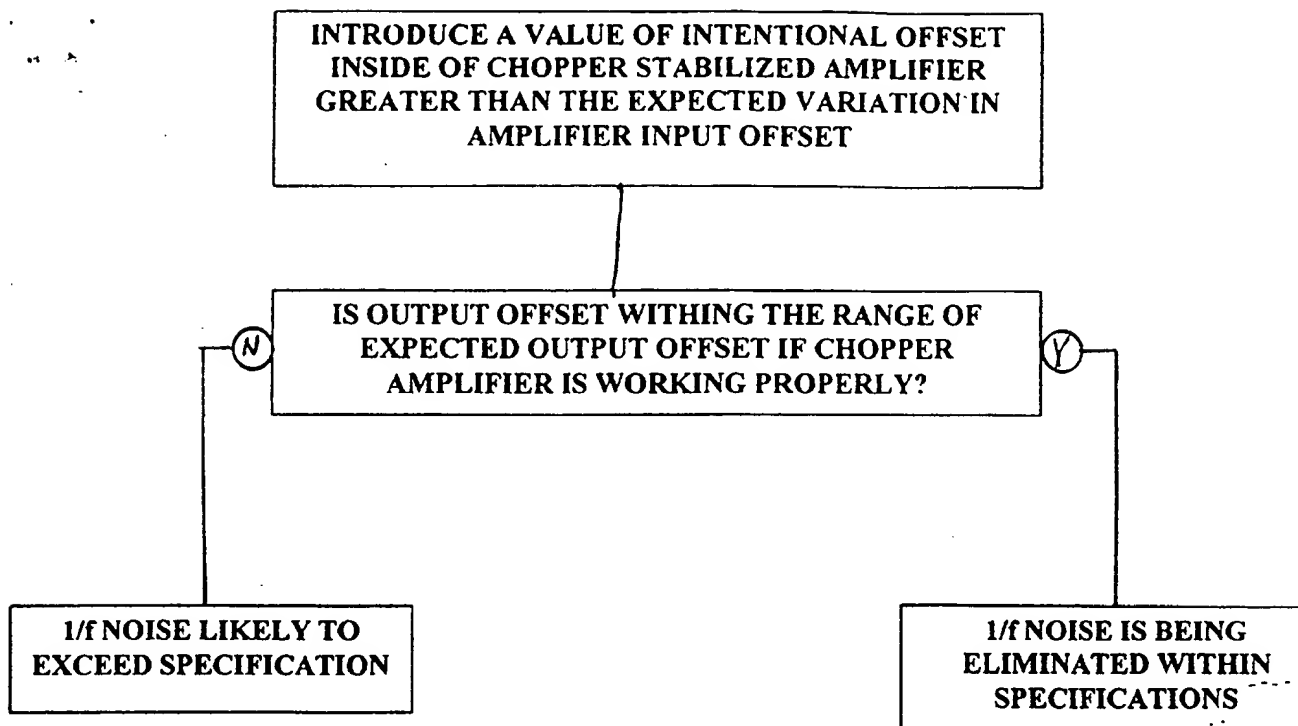


FIGURE 5.1

# Thermocouple Application

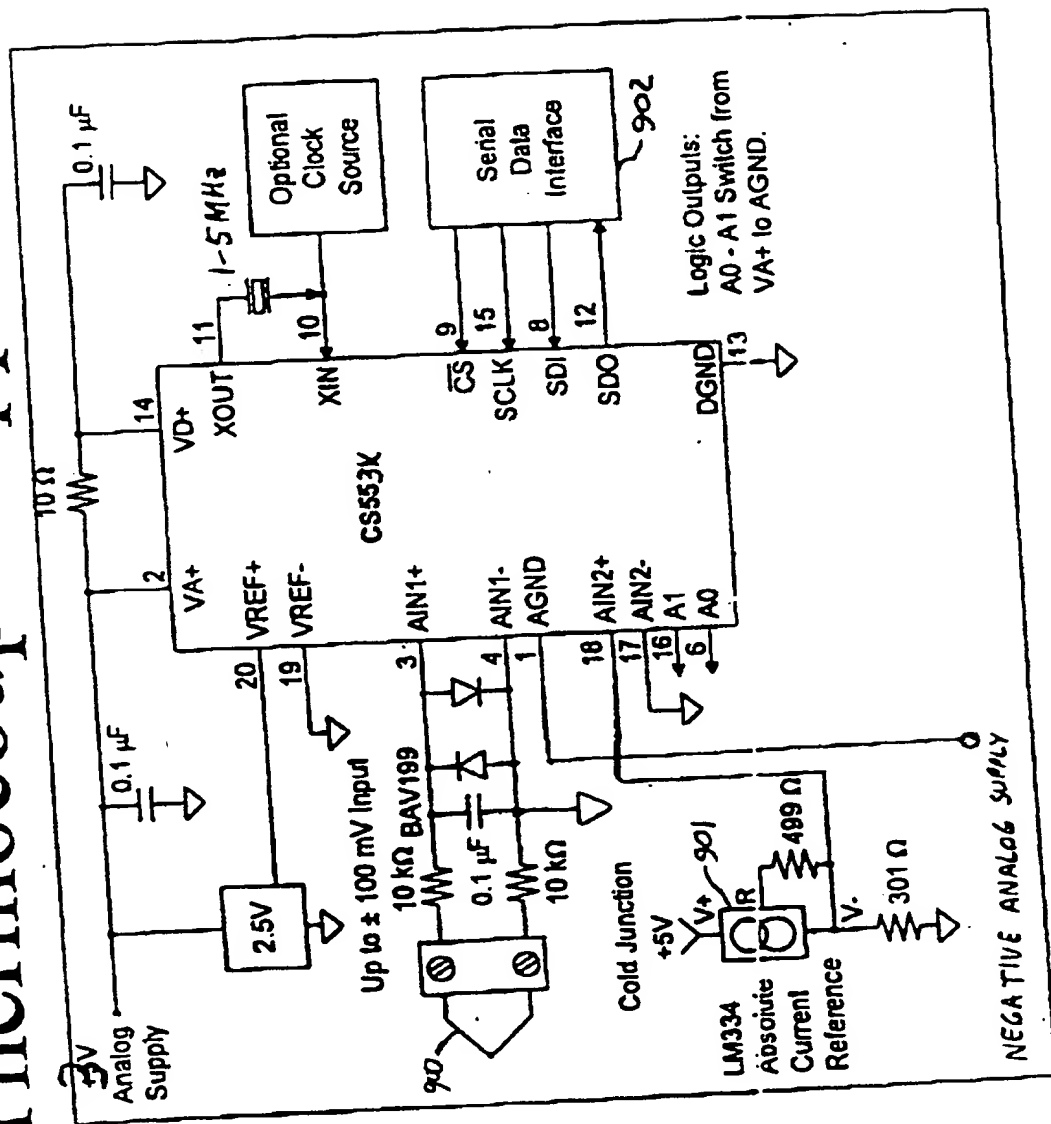


FIGURE 6.1

# Bridge Transducer Application

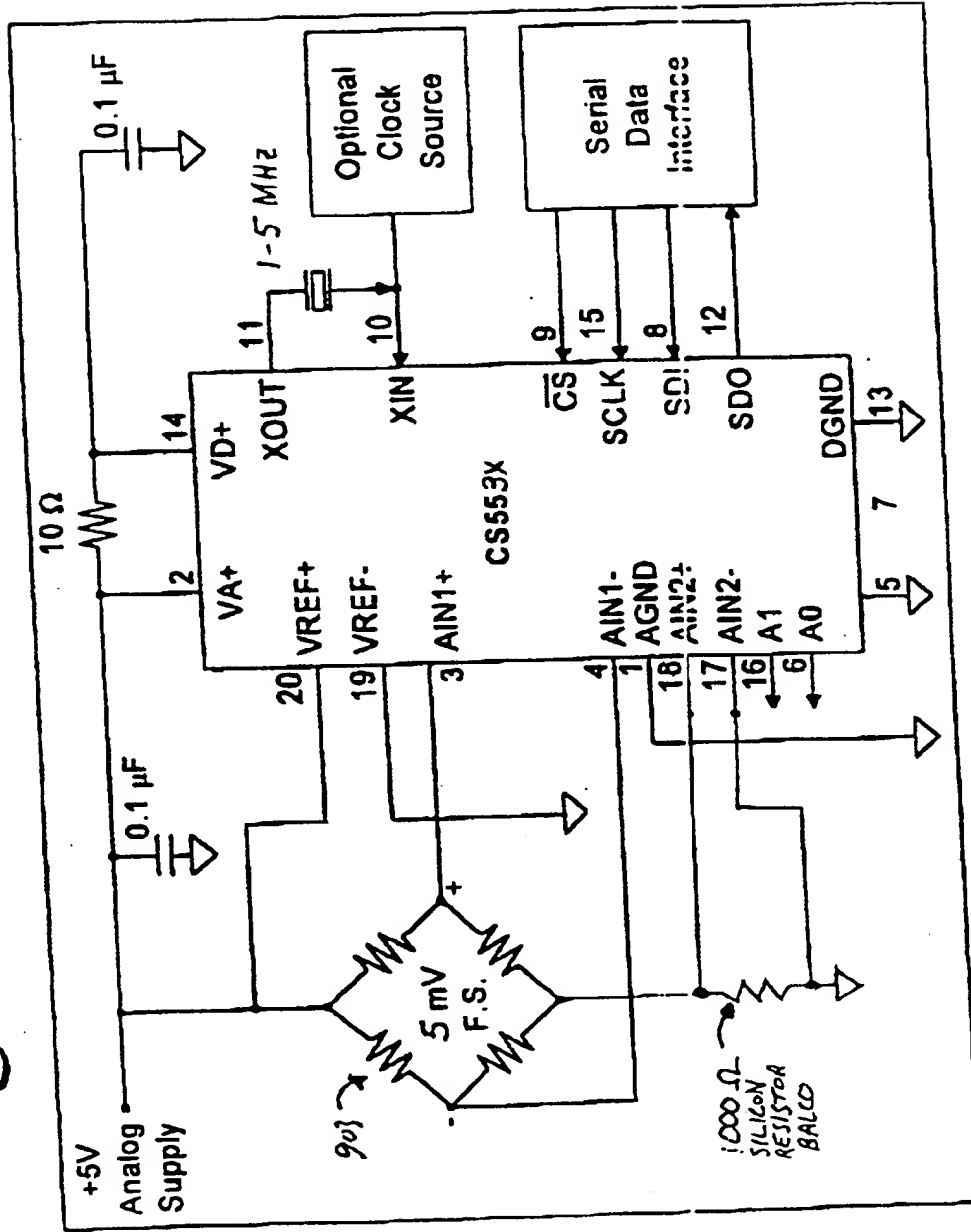


FIGURE 6.2